the process chambers and load lock chambers are connected, are claimed as extending in planes that are parallel to one another.

Summary of Rejection

The Examiner refers to the semiconductor manufacturing equipment of the present invention as being arranged in a Cartesian coordinate manner.

In rejecting claim 13, the Examiner relies primarily on the reference to Muka (USP 6,062,798). Muka discloses an embodiment of semiconductor manufacturing equipment in FIG. 2 in which the process chambers 26 – 29 and load-lock chambers 30, 31 are arranged in the so-called Cartesian coordinate manner. Muka also teaches such an arrangement **as an improvement over** the prior art cluster-type of **equipment** of FIG. 1 in which the process and load-lock chambers are **arranged in a radial or polar coordinate manner.**

Regardless of this disclosure in Muka of an embodiment of semiconductor manufacturing equipment having a Cartesian coordinate arrangement, the Examiner turns to the embodiment of FIGS. 5A and 5B in considering the patentability of the present invention. In this embodiment, the process chambers 102 and the load-lock chambers 108 are instead arranged in a polar coordinate manner. The Examiner then takes the position that it would have been obvious in view of the teachings of Yanagita et al. (USP 6,672,358) to have modified the embodiment of FIGS. 5A and